In the Claims:

Please cancel claim 2 and amend claims 1, 3-5, 7, 13, 14 and 16 as indicated below.

1. (Previously presented) An integrated device, comprising:

a plurality of functional units, wherein each functional unit is configured to receive one or more input signals, perform an operation or task, and produce one or more output signals, wherein each functional unit is configured to be inactive while one or more of the other functional units is active;

a plurality of activity detector and clock control units coupled to said plurality of functional units; wherein each activity detector and clock control unit is associated with a different one of the functional units and configured to predict when its associated functional unit will be inactive ~~for a threshold amount of time~~;

wherein a first one of the activity detector and clock control units is configured to monitor some or all of the input signals received by and output signals produced by a first one of the functional units to predict when the first functional unit will be inactive;

wherein each activity detector and clock control unit is configured to shut off a clock to its associated functional unit in response to its associated functional unit being predicted to be inactive ~~for at least the threshold amount of time~~, and provides the clock to its associated functional unit when its associated functional unit is active.

2. (Canceled)

3. (Currently amended) The integrated device as recited in claim [[2]]1, wherein the input signals received by the first functional unit comprise control signals for controlling the operation of the first functional unit, and wherein the first activity detector and clock control unit is configured to monitor one or more of the control signals to predict when the first functional unit will be inactive.

4. (Currently amended) The integrated device as recited in claim [[2]]1, wherein the input signals received by the first functional unit comprise data operated on by the first functional unit, and wherein the first activity detector and clock control unit is configured to monitor the flow of data to the first functional unit to predict when the first functional unit will be inactive.

5. (Currently amended) The integrated device as recited in claim [[2]]1, wherein the input signals received by the first functional unit comprise instructions to be performed by the first functional unit, and wherein the first activity detector and clock control unit is configured to monitor the instruction flow to the first functional unit to predict when the first functional unit will be inactive.

6. (Previously presented) The integrated device as recited in claim 1, wherein a first one of the activity detector and clock control units is further configured to determine if its associated functional unit has been inactive for a threshold amount of time; wherein the first activity detector and clock control unit is configured to shut power off to its associated functional unit if its associated functional unit has been inactive for at least the threshold amount of time and provide power to its associated functional unit if its associated functional unit has not been inactive for at least the threshold amount of time.

7. (Currently amended) The integrated device as recited in claim [[1]]6, wherein said threshold amount of time is programmable.

8. (Previously presented) The integrated device as recited in claim 1, wherein each of the activity detector and clock control units comprises:

an activity detector configured to predict when the associated functional unit will be inactive; and

a clock gate coupled to the activity detector and configured to receive a main clock source for the integrated device and provide a functional unit clock source to the associated functional unit;

wherein the activity detector is configured to control the clock gate to shut off the functional unit clock source for the associated functional unit when the associated functional unit is inactive.

9. (Original) The integrated device as recited in claim 1, wherein a first one of the activity detector and clock control units comprises an output emulator configured to drive the output signals for a first one of the functional units to a safe state when the clock is shut off to the first functional unit.

10. (Previously presented) A microprocessor, comprising:

an integer execution unit configured to receive an integer instruction stream and execute integer instructions from the integer instruction stream;

an floating point execution unit configured to receive a floating point instruction stream and execute floating point instructions from the floating point instruction stream;

an integer activity detector unit coupled to the integer instruction stream and configured to predict when the integer execution unit will be inactive and shut a clock off to the integer execution unit in response to it becoming

inactive, wherein the integer activity detector unit is configured to predict when the integer execution unit will be inactive by predicting when no integer instructions will be presented to the integer execution unit for a threshold amount of time, and wherein the integer activity detector unit is configured to shut the clock off to the integer execution unit in response to said predicting and provide the clock to the integer execution unit when an integer instruction is presented to the integer execution unit; and

a floating point activity detector unit coupled to the floating point instruction stream and configured to predict when the floating point execution unit will be inactive and shut a clock off to the floating point execution unit when it is inactive.

11. (Previously presented) The microprocessor as recited in claim 10, wherein the floating point activity detector unit is configured to predict if no floating point instructions will be presented to the floating point execution unit for a threshold amount of time; wherein the floating point activity detector unit is configured to shut the clock off to the floating point execution unit in response to predicting no floating point instructions will be presented to the floating point execution unit for the threshold amount of time and provide the clock to the floating point execution unit when an floating point instruction is presented to the floating point execution unit.

12. (Previously presented) The microprocessor as recited in claim 10, wherein said threshold amount of time is programmable.

13. (Currently amended) A microprocessor, comprising:

an instruction fetch and decode unit configured to fetch and decode microprocessor instructions;

an instruction scheduler configured to receive an instruction stream from the instruction fetch and decode unit, wherein the instruction scheduler is further configured to buffer the instruction stream and schedule instructions from the instruction stream for execution;

an integer execution unit configured to receive integer instructions from the instruction scheduler and execute the integer instructions;

a floating point execution unit configured to receive floating point instructions from the instruction scheduler and execute the floating point instructions;

an activity detector coupled to the instruction scheduler and configured to monitor the instruction stream to predict a lack of instructions for the integer execution unit for a first threshold amount of time and to predict a lack of instructions for the floating point execution unit for a second threshold amount of time;

a first clock control unit configured to control a first clock to the integer execution unit, wherein said first clock control unit is configured to shut off the first clock to the integer execution unit in response to the activity detector predicting a lack of integer instructions in the instruction stream for said first threshold amount of time; and

a second clock control unit configured to control a second clock to the floating point execution unit, wherein said second clock control unit is configured to shut off the second clock to the floating point execution unit in response to the activity detector predicting a lack of floating point instructions in the instruction stream for said second threshold amount of time.

14. (Currently amended) The microprocessor as recited in claim 13, wherein the activity detector is configured to monitor the instruction stream to predict a lack of

floating point instructions in the instruction stream for at least [[a]] said second threshold amount of time and control the second clock control unit to shut the second clock off to the floating point execution unit in response to the activity detector predicting the lack of floating point instructions in the instruction stream for at least ~~the~~ said second threshold amount of time.

15. (Previously presented) The microprocessor as recited in claim 14, wherein the activity detector is configured to monitor the instruction stream to detect the presence of floating point instructions in the instruction stream and control the second clock control unit to restore the second clock to the floating point execution unit when a floating point instruction is scheduled for the floating point execution unit.

16. (Currently amended) An integrated device, comprising:

a first functional unit configured to receive an first input and perform a first operation or task according to the first input;

a second functional unit configured to receive a second input and perform a second operation or task according to the second input;

an activity detector ~~coupled to the first and second inputs and~~ configured to monitor some or all of the input signals received by and output signals produced by the first and second functional units to predict when the first function unit will be inactive ~~for a threshold amount of time~~ and when the second functional unit will be inactive ~~for a threshold amount of time~~;

a first clock control unit configured to control a first clock to the first functional unit, wherein said first clock control unit is configured to shut off the first clock to the first functional unit in response to the activity detector predicting that the first functional unit will be inactive ~~for at least a threshold amount of time~~; and

a second clock control unit configured to control a second clock to the second functional unit, wherein said second clock control unit is configured to shut off the second clock to the second functional unit in response to the activity detector predicting that the second functional unit will be inactive ~~for at least a threshold amount of time~~.